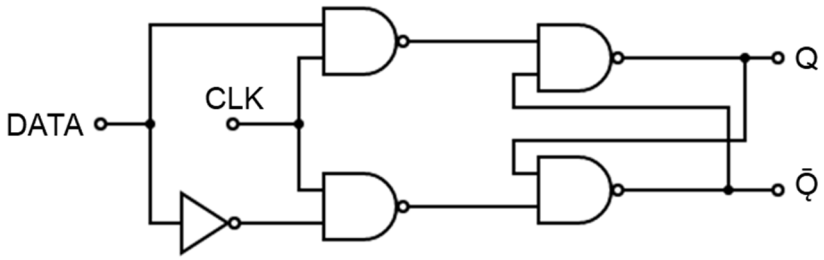
Physics 427 Lab #10

FLIP FLOPS

1. D flip flops

a) D flip flops from gates



Use four NAND gates and a NOT gate to build the D FF shown in the figure above. Connect the D (DATA) input to a wire that can be connected manually to either + 5 volts (HI) or Ground (LO), or use the data switches along the bottom of the breadboard. Connect the CLK input to another wire that can be connected manually to either + 5 volts (HI) or Ground (LO), or use another data switch along the bottom of the breadboard. Monitor the Q and $\bar{Q}$ (not-Q) outputs with the DSO or with the LEDs on the top right of the breadboard.

It may be helpful if you label the pin numbers on the 4 NAND gates in the diagram.

Verify the operation of the D FF, whose truth table is given below. In particular, verify that when the CLK is HI, Q follows D, and when the CLK is LO, Q holds the value that D had just before the CLK went LO (this is called “latching”).

Demonstrate to the instructor that your circuit works as expected.

D Flip-flop

Symbol

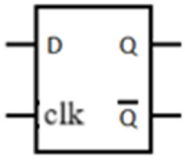


Table of truth:

clk	D	Q	$\overline{Q}$
0	0	Q	$\overline{Q}$
0	1	Q	$\overline{Q}$
1	0	0	1
1	1	1	0

b) Level-triggered D flip flops (D latch)

The 7475 IC contains 4 D latches (each one functioning like the D latch in part a). Be careful about the unusual position of the V_{cc} and Ground pins. We will use only the first latch on the chip. Connect 1D (the data input) to the TTL output of the FG and set the frequency to approximately 0.5 Hz. This is a very slow clock, which gives us plenty of time to see what's happening. Monitor the voltages of 1D (the input) and 1Q (the output) with the DSO. For the CLK (which is called ENABLE and labeled 1C), simply use a wire that can be connected either HI or LO (or use a data switch).

Verify the operation of the D latch. (Remember, it should function exactly like the latch you constructed in part a.) Q should follow D when the CLK is HI and should latch when the CLK goes LO.)

Demonstrate to the instructor that your circuit works as expected.

c) Edge-triggered D flip flops

The 7474 IC contains two Positive-Edge-Triggered D Flip Flops. The data at the 1D input is transferred to the 1Q output on the positive-going edge of the CLK. In contrast to the D latch used above, the Q output responds to the D input only on the rising edge of the CLK.

Connect the CLEAR (1CLR) and PRESET (1PRE) pins to + 5 volts. The 1D input should be connected to a wire that can be connected either HI or LO. The 1CLK should be connected to the TTL output of the FG and the frequency should be about 0.5 Hz. Observe the behavior of 1CLK and 1Q with the DSO. Use the rising edge of the CLK signal to trigger the DSO, and display only one rising edge on the DSO screen.

Verify that the FF functions as it should (i.e., data is transferred to 1Q only on the rising edge of 1CLK).

Demonstrate to the instructor that your circuit works as expected.

Bring the PRESET pin LO and see what happens. Return the PRESET to HI and bring the CLEAR pin LO. What happens?

2. JK flip flops

[Be sure to use the 74LS73 chip and NOT the 7473. The 7473 is level-triggered.]

a) The 74LS73 IC contains two JK FF's that are triggered on the falling edge (negative-going edge) of the CLK signal. These FF's are called Negative-Edge-Triggered JK Flip Flops. Watch out for the unusual locations of the V_{CC} and GND pins. Connect 1CLR to HI. Connect 1J and 1K to wires that can be connected either HI or LO, or use the data

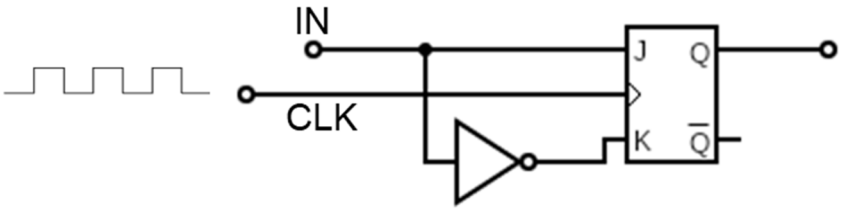
switches along the bottom of the breadboard. Connect 1CLK to the FG TTL output with the frequency set to 0.5 Hz. Use the DSO to observe 1CLK and 1Q. Use the falling edge of the CLK signal to trigger the DSO, and display only one falling edge on the DSO screen.

Verify that the FF functions as indicated by the state table given below.

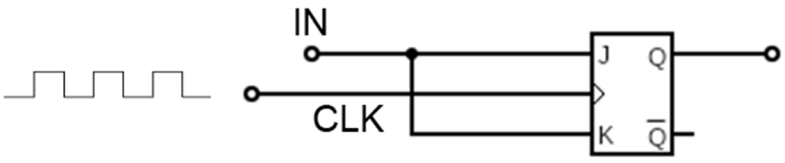
J	K	Q
0	0	Q_n
1	0	1
0	1	0
1	1	$\bar{Q}_n$

See what happens when 1CLR is brought LO. Return it to HI so that the FF will function properly.

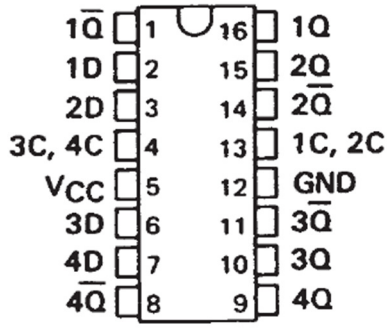
b) Connect the JK FF as shown below, and use the DSO to verify that it operates as a Negative-Edge-Triggered D FF.



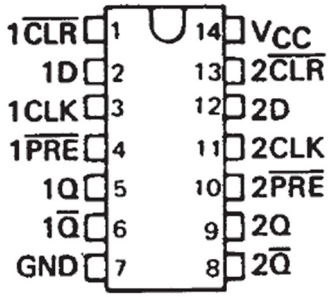
c) Connect the JK FF as shown below. This is called the <u>"toggle" configuration</u>. When the input is HI, the output changes on every falling edge of the CLK signal. When the input is LO, the FF holds the last state. Verify that the FF functions as a Toggle FF. With the input held HI, increase the CLK frequency to several Hz and observe the CLK and Q signals on the DSO. Can you see why this is sometimes called a "divide-by-two" circuit?



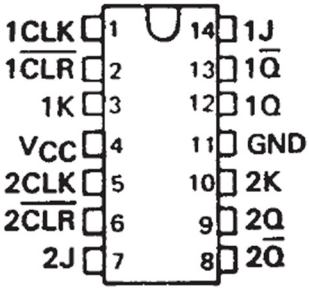
SN5475, SN54LS75 . . . J OR W PACKAGE
SN7475 . . . N PACKAGE
SN74LS75 . . . D OR N PACKAGE
(TOP VIEW)



SN5474 . . . J PACKAGE
SN54LS74A, SN54S74 . . . J OR W PACKAGE
SN7474 . . . N PACKAGE
SN74LS74A, SN74S74 . . . D OR N PACKAGE
(TOP VIEW)



SN5473, SN54LS73A . . . J OR W PACKAGE
SN7473 . . . N PACKAGE
SN74LS73A . . . D OR N PACKAGE
(TOP VIEW)



LAB REPORT **Name** _____

Physics 427 Lab #10

FLIP FLOPS

Attach notes from the lab procedure.

Answer the following questions on a separate sheet:

1) What are the major differences between the 7475 and 7474 flip flops?

2) What functions do the 7474's PRESET and CLEAR perform?

3) What are the major differences between edge-triggered D flip flops and JK FF's?

4) Show how you would construct a divide-by-4 circuit using JK FF's.

5) Describe the output of the following circuit: