Physics 427 Lab #8

DIGITAL LOGIC GATES

1. Truth tables for digital logic gates

For each of the 6 digital logic gates listed below, determine the output states of its truth table. You may use the LED displays on the breadboard to test the HI or LO of the output of a gate.

When inserting an integrated circuit (IC) into the breadboard, carefully position the chip so that it straddles the center channel of the breadboard and so that its pins are all centered in sockets of the board. Then press down gently until you feel the chip seat itself in the breadboard. Make sure that none of the pins are bent. To remove a chip, always use the plastic tweezers to gently loosen the chip and then lift it out of the breadboard.

Make sure that each chip has power by connecting it to +5 VDC and ground. For the chips we are using today, pin 14 is connected to +5 VDC and pin 7 is connected to ground (see the diagrams on the diagram page). Anytime you insert an IC into a breadboard you must connect it to these power supply voltages.

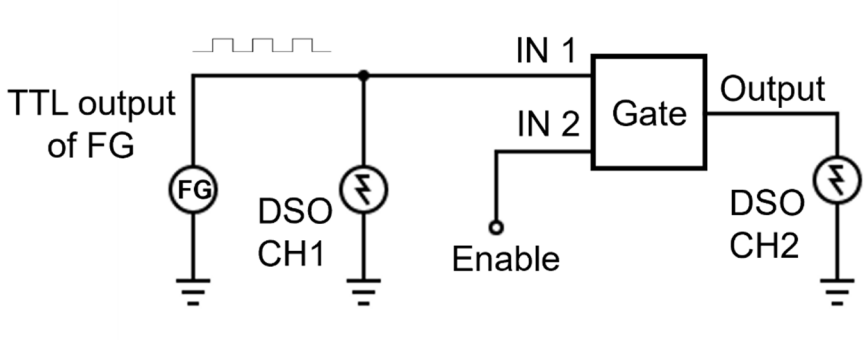
Pay special attention to the NOR gate (7402), whose input pins are pin 2 and pin 3, while its output pin is pin 1.

a) Two-input NAND (7400)
b) Two-input NOR (7402)
c) One-input NOT (7404)
d) Two-input AND (7408)
e) Two-input OR (7432)
f) Two-input XOR (7486)

When an input is “floating” (i.e., not connected to anything), does it act as a HI or LO input?

2. Data transmission gating

For each of the 5 digital logic gates used in section 1 (excluding the NOT gate), construct the following circuit:



Use the DSO CH1 to monitor the TTL output signal of the FG. It should be a square wave between 0 and 5 V, while its frequency does not matter now. The TTL output signal of the FG, going into IN1, serves as the **DATA** input of the gate. IN2 of the gate is the **ENABLE** input. Determine whether the input data is transmitted to the output when the ENABLE is HI (+5 VDC) or LO (ground). In other words, is the gate ENABLE active HI or active LO?

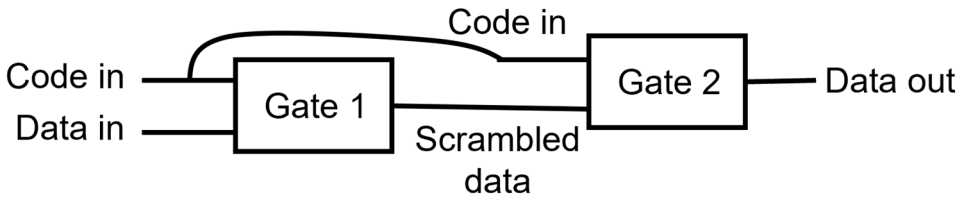
When the gate is enabled, is the output data in phase with the input data or inverted?

Describe the gate output when data transmission is disabled (is the output HI or LO?).

3. Scrambling/Unscrambling a data signal

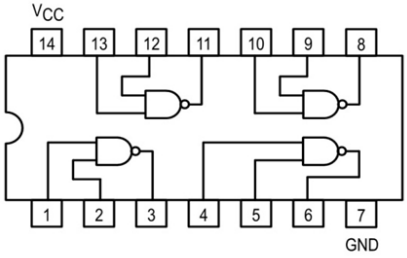
One (and only one) of the fundamental digital logic gates (AND, OR, NOR, NAND, XOR, and XNOR) can be used to scramble data and later to unscramble it. As shown below, the data is input to the first gate along with a code signal. The output data from the first gate will be scrambled (i.e., it will bear no recognizable relationship to the input data). If the scrambled data is input to the second gate along with the same code signal that was used to do the scrambling, it will emerge from the second gate in its original (unscrambled) form.

Design and construct a scrambling/unscrambling system as shown below. Use the TTL output from the FG, with a frequency of about 2 Hz, as the code signal. For the data, simply use a wire that can be connected to HI or LO.

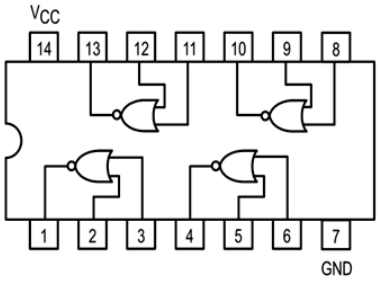


Use three LED displays on the breadboard to monitor the code, the scrambled data, and the final output data. Demonstrate to the instructor that the system works.

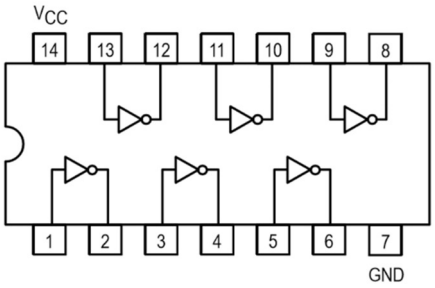
74LS00 NAND Gate



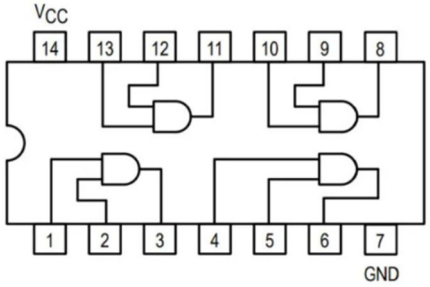
74LS02 NOR Gate



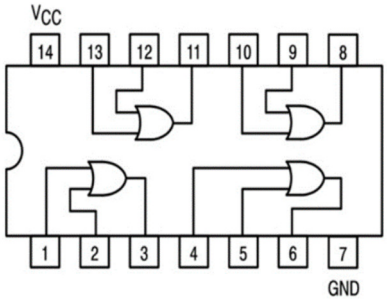
74LS04 Inverter



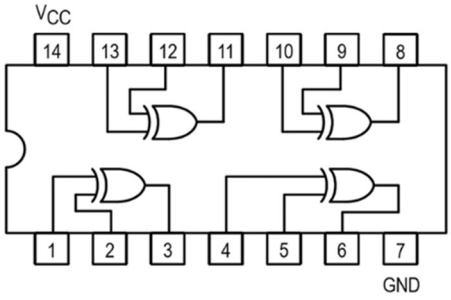
74LS08 AND Gate



74LS32 OR Gate



74LS86 XOR Gate



LAB REPORT **Name** _____

Physics 427 Lab #8

DIGITAL LOGIC GATES

1. Truth tables for digital logic gates

Give the truth tables that you determined for each of the logic gates used. In the tables, 0 = connected to ground, 1 = connected to +5 VDC.

a) NAND gate (7400)

INPUT 1	INPUT 2	OUTPUT
0	0	
1	0	
0	1	
1	1	

b) NOR gate (7402)

INPUT 1	INPUT 2	OUTPUT
0	0	
1	0	
0	1	
1	1	

c) NOT gate (7404)

INPUT	OUTPUT
0	
1	

d) AND gate (7408)

INPUT 1	INPUT 2	OUTPUT
0	0	

1	0	
0	1	
1	1	

e) OR gate (7432)

INPUT 1	INPUT 2	OUTPUT
0	0	
1	0	
0	1	
1	1	

f) XOR gate (7486)

INPUT 1	INPUT 2	OUTPUT
0	0	
1	0	
0	1	
1	1	

Based on your observations, do floating inputs act as HI or LO inputs?

2. Data transmission gating

For each of the gates used in this section, give the ENABLE state that permits data to be transmitted, the phase of the output data relative to the input data (in-phase or inverted), and describe the gate output (HI or LO) when data transmission is disabled.

Gate	ENABLE	Output Phase	Output of Disabled Gate
	(Active HI or LO)	(In-phase or Inverted)	(HI or LO)
NAND			
NOR			
AND			

OR			
XOR			----------
			----------

3. Scrambling/Unscrambling

Which logic gate did you use for this part? Show how you determined which gate to use.

Use Boolean algebra to show why only this gate will work.